A Microelectrode/Microelectronic Hybrid Device for Brain Implantable Neuroprosthesis Applications

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***Abstract*—We have designed, fabricated, and characterized a microminiaturized "neuroport" for brain implantable neuroprosthesis applications, using an analog CMOS integrated circuit and a silicon based microelectrode array. An ultra-low power, low-noise CMOS preamplifier array with integral multiplexing was designed to accommodate stringent thermal and electrophysiological requirements for implantation in the brain, and a hybrid integration approach was developed to fabricate a functional microminiaturized neuroprobe device. Measurements showed that our fully scalable 16-channel CMOS amplifier chip had an average gain of 44 dB, bandwidth from 10 Hz to 7.3 kHz, and an equivalent input noise of approximately 9 μV_{rms} with an average power consumption per preamplifier of 52 μW, which is consistent with simulation results. As a proof-of-concept demonstration, we have measured local field potentials from thalamocortical brain slices of rats, showing oscillatory behavior with an amplitude about 0.5 mV and a period ranging 80–120 ms. The results suggest that the hybrid integrated neuroport can form a prime platform for the development of a next level microminiaturized neural interface to the brain in a single implantable unit.**

***Index Terms*—Brain computer interface, integrated neural probe array, low-noise preamplifier, neuroprosthesis.**

I. Introduction

THERE have been striking advances in the past two years in the development of recording techniques that have enabled the extraction of signals from the living brain to control rudimentary robotic devices [1], [2]. The approach involves intracortical sensors in the form of microelectrode arrays that are placed very near neuron cell bodies. For example, the development of such a brain-machine recording interface for the motor cortex (MI) has enabled the laboratory demonstration of "thoughts-to-action" observations in macaque monkeys [1]. It now appears likely that comparable recording access will be applied to the living human brain in the near future, propelled in part by the need to develop a practical neuroprosthetic interface for paralyzed patients.

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Among the several different approaches to the multielectrode sensor development, a silicon-based monolithic unit with up to 100 Pt/PtSi coated electrodes has been particularly successful in sampling the neural activity in the MI [3], [4]. Chronically implanted, this multielectrode arrangement allows the long term (>1 year) exploration of a significant amount of motor cortex space so that, in conjunction with newly developed decoding techniques using probabilistic analysis [5], good correlation has been achieved for the arm movement of a monkey between the signals recorded directly from the brain ("thought-for-action") and the real physical action by the animal [2]. On the other hand, multielectrode sensors, whether silicon or microwire based, presently require cumbersome, complex cabling arrangements with a significant amount of physical wiring for the "spike signals" to reach the extracranial amplifier and signal processing electronics. Conventionally, the amplifiers are mounted on headstages literally screwed to the skull and connected by multiconductor cable to rack-mounted electronics for capture and storage. At the moment, the total system, with electronics on a rack scale, is not compatible with any degree of meaningful portability. Yet portability is highly desirable and can be viewed as a prime goal for fulfilling the future promise of a still embryonic neuroengineering technology.

While a number of efforts are underway to compact the sensing instrumentation associated with the development of a real-time brain machine interface [6]–[8], we show here first steps of a successful integration and operation of a chipscale unit that integrates a silicon-based multielectrode array with an ultra low power, high performance silicon microelectronic integrated circuit. This monolithic unit whose details will be described below has been applied in an *in vitro* test bed situation to measure electrical activity from rat brain slices. The CMOS integrated circuit contains an array of sixteen low-noise preamplifiers with on-board multiplexing and an output buffer amplifier that enable a significant reduction in the amount of wiring which is required to extract the neural signals from the implanted recording unit for subsequent processing and analysis. The amplifier array is bonded directly to a silicon electrode array and then is wire-bonded to a 7-wire interface and encapsulated with silicone. We believe that our hybrid unit represents a first of its kind and, more important, view this accomplishment as a prime platform for the development of a next level of microminiaturized "neuroports" where eventually all required electronics will be part of a single brain-implantable unit.

Specialized CMOS devices for neural signal capture and preprocessing have seen extensive prior development. The first successful effort to integrate amplifiers with a sensor probe that we are aware of was presented by Najafi and Wise [9] in 1986 and

that line of development has continued to the present [8], [10]. This paper is based on needle-like silicon blades with side contacts built using anisotropic etching. The CMOS circuitry is at one end of the assembly. Signals from several sites along the blade are multiplexed into a smaller set of amplifiers that in turn multiplex to one output. Noise levels down to 11 $\mu\mathrm{V_{rms}}$ referred-to-input have been reported with per-amplifier power levels around 100 $\mu\mathrm{W}$. In our applications, a planar array of electrode needles is more attractive for implantation and the need for continuous amplification in all channels places a more stringent restriction on power dissipation that makes achieving low input noise levels more difficult.

In a CMOS amplifier, one can show that the input-referred thermal noise and power dissipation are inversely related such that the product of noise voltage squared times the power should be constant for a given circuit topology. The best reported value of this quality factor is for a circuit presented by Harrison [11], [22], which showed 2.4-$\mu\mathrm{V_{rms}}$ noise with 80 $\mu\mathrm{W}$ per amplifier. It used integrated capacitive coupling on its inputs and floating, high-value resistors based on optimized P-MOSFETS. However, this circuit was not designed for use attached to an electrode array and its power dissipation does not include what would be required for multiplexing. It also had some dc baseline drift. Recently, Mojarradi and coworkers [12] presented a design that, like our system, is to use an amplifier array bonded to a set of electrodes. Once completed, their system will rely on an elaborate digital-feedback correction method for dc offset and will incorporate more digital elements on the same integrated circuit as the amplifiers. (Their results did not show an integrated functional system). More recently, efforts at Duke University have been presented by Obeid, *et al.* [7] for integrated circuits to make very small and efficient hybrid head stage systems by incorporating all amplification and filtering operations for 16 channels into single chips. They use discrete capacitors for dc blocking on the inputs and achieve noise levels of 4.4 $\mu\mathrm{V_{rms}}$ for 217-Hz high-pass filtering at gains of 47–53 dB and power dissipation of 950 $\mu\mathrm{W}$ per channel. Because of high power dissipation, these circuits could not be readily adapted for implantation.

This paper is organized as follows: In Section II, the design and performance of the low power silicon integrated preamplifier and multiplexing circuit is described. This is followed in Section III by a description of the approach and implementation of the integration of the multielectrode array with the CMOS chip. The characterization and performance of the hybrid neuroprobe is presented in Section III, including comments on the issues of encapsulation. Finally, Section IV provides a summary of this work and offers a technological outlook about the future of these emerging neuroengineering concepts.

II. A CMOS Integrated Preamplifier Array With Integral Multiplexing

Fig. 1 shows the overall architecture of the CMOS amplifier array. There are 16 preamplifiers $(0, 1, \ldots \mathrm{F})$, each with an input bonding pad within its own area of the integrated circuit, in a 1.6 mm $\times$ 1.6 mm square array. The array pitch of 400 $\mu\mathrm{m}$ exactly matches that of the array of extracellular electrodes so that bonding each input pad to its corresponding electrode can be done by epoxy ball bonding as described in Section III. Each amplifier also has a CMOS transmission gate switch attaching its output to a column line under control of a row select line. Amplifier outputs are routed to the output buffer amplifier by row and column selection implemented with a digital row decoder and an analog column multiplexer also based on CMOS switches. A total of only seven wires is needed as the interface to the chip, including four source select lines, output, power, and ground. The circuit was fabricated on a 2.2 mm $\times$ 2.2 mm chip in the AMIS 1.5-$\mu\mathrm{m}$ process through the MOSIS service.[1]

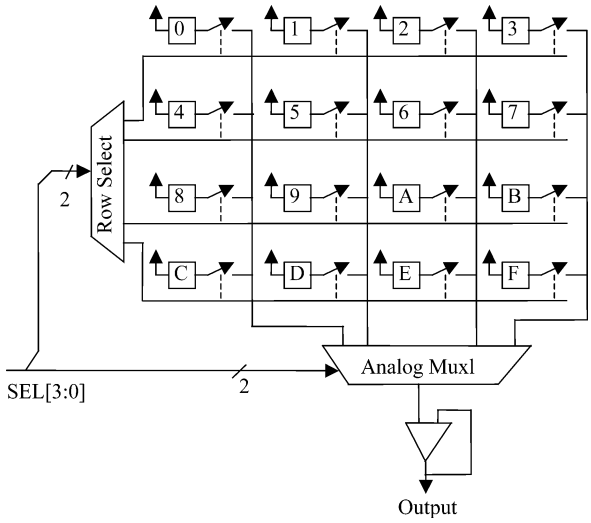

Fig. 1. Block diagram of a CMOS integrated preamplifier array with row and column analog multiplexing and unity gain output buffer.

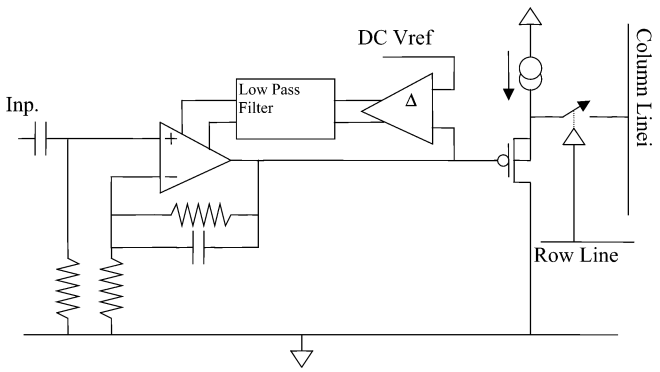

Fig. 2. Block diagram of an individual preamplifier. The symbol Δ denotes a low-gain differential amplifier.

The components of an individual preamplifier are shown in Fig. 2. An operational amplifier using a folded cascode circuit with P-channel input transistors and a source follower output buffer provides signal amplification. The noninverting input of that amplifier connects through an resistance–capacitance (*RC*) high-pass network to the sensing electrode that the amplifier services. This resistor is actually a diode-connected N-channel MOSFET and the capacitor is a double polysilicon structure underneath the bonding pad. The MOSFET in this position provides very high resistance for small signal inputs, sufficient nonlinearity to speed recovery from overload, and a limited measure of electrostatic discharge protection. Gain and high-frequency

[1][Online]. Available: www.mosis.org.

cutoff are set by a pair of resistors and another polysilicon capacitor in the feedback path. To achieve very large values of resistance in a reasonable area, these feedback resistors were also built with N-MOSFETs, but a circuit that applies a portion of the signal to the gate of one feedback transistor linearizes that resistance to allow its use with large signals. The design target for high-frequency cutoff was 7.5 kHz.

A separate dc compensation feedback loop sets the bias levels for the amplifier. Because the input *RC* network and the main feedback network both set the dc levels of their respective operational amplifier input terminals to near 0 V while the power supply is a single ended 3.3-V supply, it is necessary to use active feedback to imbalance the first stage slightly, thus setting the output dc level near 1.5 V. A low-gain differential amplifier (marked "Δ" in Fig. 2) computes the difference between the output of the operational amplifier and its desired dc reference level. This difference signal is low-pass filtered at a very low (sub-Hertz) cutoff frequency and converted to a current by a P-channel differential pair. The filter is implemented with transistors in deep subthreshold operation in a circuit similar to those used by Najafi and Wise [9], [13]. The filtered output current adds to the drain currents of the operational amplifier input transistors, introducing a small imbalance in the first stage that compensates for any input transistor imbalance and for the dc difference between the inputs and the output of the OP amp.

To isolate the operational amplifier from the effects of the switch connecting the preamplifier to its output column line, there is a P-channel source follower stage implemented in an isolated N-well. Without such isolation, the operational amplifier output would be subject to stepwise disturbance by the inrush current charging the column-line capacitance at the onset of row selection. Since the amplifier bandwidth is relatively narrow to minimize noise and to prevent aliasing, this disturbance would not settle in time for analog to digital conversion. The output impedance of a source follower is low enough (on the order of $1/g_m \propto 1/I_D$) to make the column line settle quickly without feedback. Connecting the isolation well in which the follower transistor is built to the source of the transistor and using constant current biasing make the stage linear. To conserve power, the bias currents of these followers are only turned on slightly before and during row selection, being controlled by the row select multiplexer.

The principal requirement on the output buffer amplifier is that it should settle to 12-bits in under 1 ms so that the ADC converter can operate at a full 640 ksps rate. The target settling time was 650 ns to allow its use in a scaled up version of the system and this goal is met in simulation. The analog to digital converter used in the test system was an Analog Devices AD7495 (The input capactance switches between 6 and 20 pF at the sampling rate on a roughly 60% duty cycle.) Because its input capacitance is part of its sampling circuit, a common practice in low-power, high-speed ADCs, that capacitance is both relatively high (about 20 pF) and time dependent. The buffer amplifier must be able to drive this load with adequate output current for fast slewing, adequate bandwidth for settling, and no instability on stepwise changes in load. It is also necessary that the amplifier bias current be kept low to minimize power dissipation. The buffer is an operational amplifier connected for unity gain. Its first stage is an N-channel differential pair and the second stage is a class AB output stage of a form introduced by Duisters and Dijkmans [14]. In simulation it achieves a slew rate of $1 \cdot 10^7$ V/s, a small signal bandwidth of about 7 MHz and stability over a wide range of load capacitance.

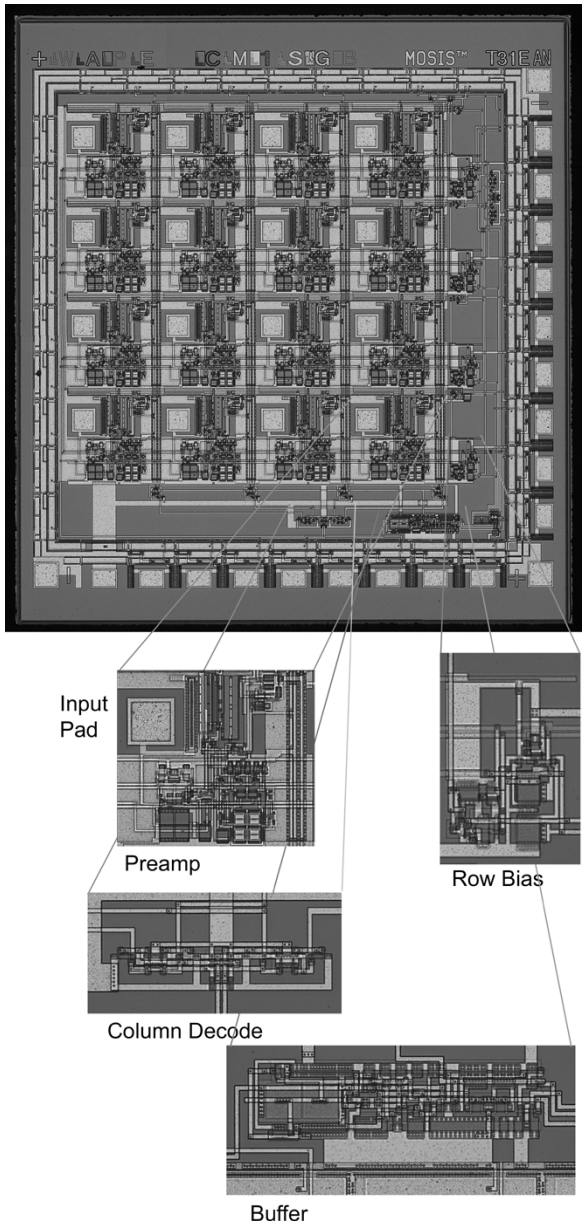

Fig. 3. Photomicrograph of the integrated circuit showing preamplifier array, multiplexer components, and buffer.

Fig. 3 is a photomicrograph of the chip showing the relative size and placement of each of its principal components. In the present design, the current through an external resistor sets bias currents for all sections of the circuit. That current is copied and distributed to current mirrors on the end of each amplifier row to provide biasing across the row. The external resistor will eventually be replaced by an on-chip constant transconductance bias circuit. The entire design is highly modular and is easily scalable to larger arrays as the technology for suitable packaging develops. For example, the row bias networks were designed to be extended without change to service ten preamplifiers. The micrograph shows the standard analog bonding pads used for external connections around two edges of the die. There are power and ground distribution nets just inside the pad frame that are

implemented as two metal rings surrounding the active circuitry. Inside those frames is a substantial band of open area for multiplexer and buffering circuitry between the power network and the amplifier array.

The target applications of this sensor require measuring both action potentials or "spikes" and local field potentials, which imposes stringent requirements for both noise and bandwidth. At the same time, implanting the sensor requires care in setting power dissipation to be compatible with minimal tissue damage over very long term use. Spike activity detected with extracellular electrodes of our type is typically in the range of 90 to 120 μV_{P-P} and spike duration is such as to require a high-frequency -3-dB cutoff of around 7.5 kHz to preserve the waveshape. Typically the Pt/PtSi electrode tips over silicon electrodes show impedances *in vivo* with resistive parts in a range of 150 to 300 $k\Omega$, and this corresponds to Johnson thermal noise in the input signal of approximately 5 μV_{rms}. Local field potentials are much higher amplitude and require an input dynamic range that accommodates at least 4 mV_{P-P}. The time scale of local field potentials is relatively much slower than that of spikes and requires a frequency response down to around 10 Hz. A much lower frequency cutoff than 10 Hz may lead to baseline drift from changes in unmatched half-cell potentials at the electrodes that may compromise dynamic range.

Our design choices were most heavily constrained by power considerations, which suggested the need to be as near to 50 μW per amplifier as practical so that a scaled-up version would present acceptable thermal loading of the tissue in contact with it (Our worst-case thermal model was single-sided heat removal through still water with no heat transport by blood circulation. We constrained ourselves to a power level that would give approximately a 1 °C emperature rise at the center contact point of the device). Only 60% of amplifier power was allocated to the input operational amplifier, the remainder being used for biasing, multiplexer drive capability, and dc stabilization circuitry. The use of just 30 μW in the first amplifier stage automatically limits the available signal-to-noise ratio due to themal noise in the input pair. The dc compensation circuitry used 12 μW, and, with its difference amplifier and the current that it injects into the first amplifier stage, it has two undesirable effects: it raises power consumption by 20% and it further raises the noise level by about 1.7 dB. Its main purposes are to stabilize the output bias level to make the output circuitry easier to design and to relieve requirements on the ADC circuitry. With these compromises, simulation still showed an overall noise level of only slightly over 5 μV_{rms}, which would result in a system with roughly a 3-dB noise figure.

Fig. 4 and Table I summarize the principal performance parameters of the final design. The measured frequency response from the Bode plot of Fig. 4 has -3-dB cutoff points at 10 Hz and 7.3 kHz, and the phase shift at those frequencies is compatible with approximately single pole behavior at both ends of the range. The low-frequency cutoff point is adjustable by an external voltage to P-MOSFET devices in the low-pass filter in the dc compensation circuitry. The maximum gain is 44 dB. Table I shows the results of SPICE simulation of the amplifier circuitry compared to the measured results. The aggregate noise was measured to be 9 μV_{rms} referred-to-input from the standard deviation of 0.5 s of 40 ksps data taken in saline solution and including thermal noise from the probes as discussed below. This

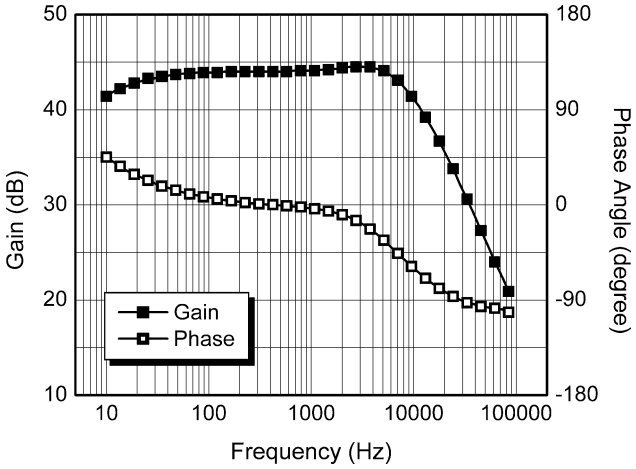

Fig. 4. Bode plot of the response of one channel of the amplifier IC.

TABLE I
SIMULATED AND MEASURED PERFORMANCE OF THE AMPLIFIER IC

Parameter	Simulation	Measurement
Noise (RTI)	6.8 μV_{RMS}	9 μV_{RMS}
Power per amplifier	52 μW	N/A
Power	1.3 mW	1.4 mW
High frequency cutoff (-3 dB)	7.5 kHz	7.3 kHz
Low frequency cutoff (-3 dB)	5 Hz	10 Hz
Overload recovery (200 mV step)	N/A	745 ms

compares to a simulation result of 6.8 μV_{rms} for the preamplifier alone and 8.8 μV_{rms} with a 200 $k\Omega$ resistive source. An alternative measure of noise that is relevant to the detection of action potential activity (spikes) is the peak-to-peak noise of suitably filtered data in a quiescent measurement. We have measured 50 μV_{P-P} noise in 0.5 s of data taken with the probes in artificial cerebrospinal fluid (ACSF) saline using a high-pass, equiripple, 164-tap finite impulse response digital filter having a stopband with 40-dB attenuation below 300 Hz and a passband above 600 Hz. We are continuing the development of this circuit to simplify biasing requirements, and results describing the circuitry will be published elsewhere.

Finally, we wished to determine if the input *RC* coupling and dccorrection circuits achieved the goal of a stable mean output level independent of any dcoffset in the signal. For this measurement we applied a 0.2 V_{P-P} square wave at 0.5 Hz to the input and measured the recovery from overload. Recovery was somewhat asymmetric with polarity, but the worst case was 212 ms for the circuit to come out of saturation and 750 ms total to reach within a few millivolts of the final equilibrium dc level.

III. Integration of the Multielectrode Array With CMOS Chip: A Hybrid Neuroprobe and Performance Evaluation

Integration of heterogeneous components is an important and difficult challenge in modern micro-and opto-electronics. In the case of the silicon-based multielectrode neural sensor array and the CMOS microelectronic integrated circuit chip, one faces specific difficulties because of the contrasting geometries and materials. For example, the extreme fragility

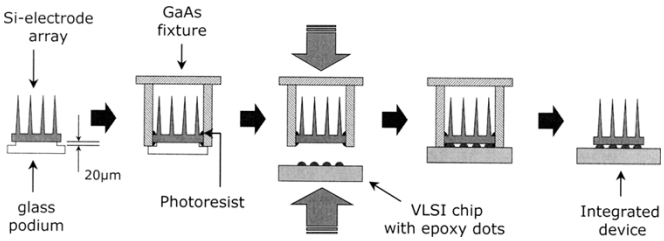

Fig. 5. Assembly sequence for electrode to amplifier connection, showing the use of a temporary holding fixture.

of the silicon-based electrode array and differences of the thermal coefficients of expansion between the components to be bonded together place constraints on the packaging that are quite stringent and specific to the problem at hand.

We have chosen to use a flip-chip integration strategy based on a carefully chosen conductive epoxy for the the electrical interface between the electrode array and the CMOS chip. This approach has two advantages: first it limits the stresses of pressure and temperature on the base of the electrode array and second, it eliminates the stress that soldering or ultrasonic bonding would place on the double polysilicon input capacitor structure of the chip, increasing its reliability. As shown in Section II (Fig. 3), the CMOS chip which we have developed for testing purposes is a 16 channel device so that the corresponding number of microelectrodes need to be electrically connected to the appropriate bonding pads on the chip simultaneously. Conductive silver epoxy (Epotek Model H20E-PFC) is applied to the pads $(80\ \mu\mathrm{m} \times 80\ \mu\mathrm{m})$ of the CMOS chip by a pin stamping technique with a programmable epoxy dispenser (Microassembly Technologies, Ltd. Model 6495), so that approximately 150-μm diameter and 50-μm high epoxy dots are deposited with 20 μm placement precision. An important issue was the choice of epoxy of the right thixotropic properties so that the correct size dots were formed that would also flow properly without excessive pressure on assembly.

The 16 element microelectrode arrays were bonded to the CMOS chip by using a high accuracy, manual flip chip and die bonder (RD Automation Model M9A). We employed 4×4 arrays from the Bionic Technologies Division of Cyberkinetics Inc., with electrode heights varying from 0.5 to 1.5 mm. The flip-chip bonding equipment employs a high-resolution optical guiding system for alignment of two parallel surfaces with micrometer precision. A key step was to develop a specialized holder for the microelectrode arrays, both to keep their fragile electrodes from breakage as well as to facilitate the optically-based alignment and leveling. The principal steps in the process flow are summarized schematically in Fig. 5. The electrode set is first placed on a glass podium, the height of which ultimately fixes the deformation and finished height of the epoxy posts that connect the electrodes to the amplifiers. Then a fixture made from GaAs plates is built around the electrodes using Shipley 1800 series photoresist as an adhesive. The two side plates in the fixture have identical heights since they were cut from a single original piece. That piece had exactly parallel sides since it was cleaved along the crystalline orientation planes of GaAs and eventually provided excellent parallelism between the base of the Si microelectrode array and the top surface of the VLSI chip. When the resist has set properly, the fixture is transferred

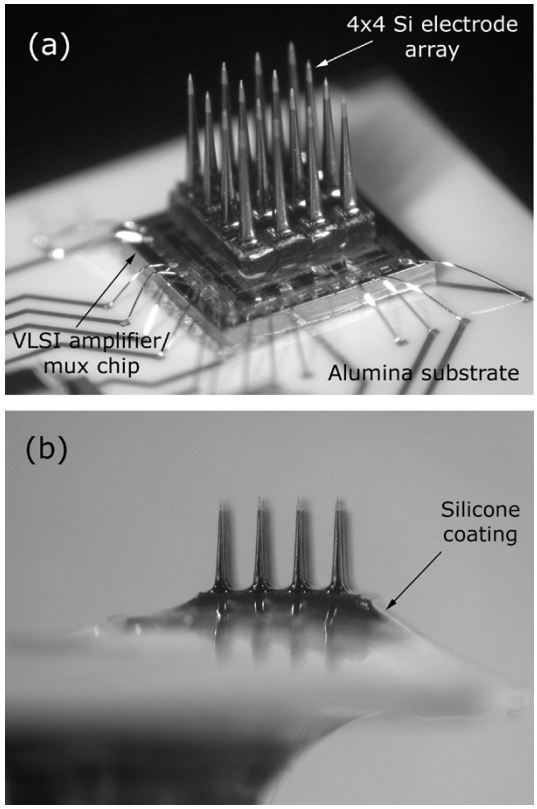

Fig. 6. Electrode and amplifier assembly prior to (a) and after (b) silicone encapsulation.

to the flip chip bonder where its gold base pads are aligned with the pin-stamped epoxy dots on the amplifier integrated circuit (IC) chip. The two parts are brought together slowly to a final bonding pressure of 0.5 kg, most of which is absorbed by the fixture side plates. It leaves about 20 μm gap between the two parts predetermined by the height of the glass podium. Finally, the epoxy is cured at 100 °C for 90 min, after which the fixture is removed with acetone.

For test purposes, we attached the hybrid neuroprobe by conductive epoxy to a 0.25-mm-thick alumina support plate with patterned thin film gold wiring to connect it to the rest of the system electronics and optoelectronics. We employed 1 mil Al-1% Si bonding wires from the CMOS chip to bonding pads on the alumina plate, which in the present implementation also carried several surface mount passive electrical components, mainly for setting the proper electrical bias conditions for the amplifier chip. *It is important to note that the integration approach is fully scalable to large microelectrode arrays (100 recording channels and beyond) and that the choice of a 16 channel system was made for test development purposes only.*

The hybrid assembly was washed in acetone, air-dried, and primed with a naptha borne silicates-titanate-silane primer (NuSil CF2-135). After the primer dried, the assembly was underfilled and then overcoated with four coats of silicone elastomer (NuSil MED 6015). The silicone was applied by brush to avoid contaminating the electrodes. After each coat the silicone was cured at 100 °C for 1 h. To fill any pinholes an overcoat of 40% nitrocellulose, 40% toluene sulfonamide formaldehyde, and 20% dibutyl phthalate in an alcohol-acetate-toluene solvent was applied by brush. This sealant was adequate for short term

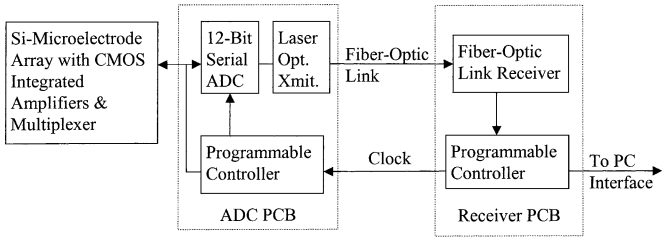

Fig. 7. Block diagram of the signal processing system used to capture data from the sensor. Dividing the system into two subsystems on separate boards allows testing technologies for optical power and data return.

use but will require improvement for *in vivo* use. Fig. 6 shows a photographic view of the hybrid integrated unit prior to and after the silicone encapsulation.

The integated encapsulated assembly, supported mechanically by the alumina plate, was subsequently mounted to a thin aluminun rod attached to a micromanipulator that enabled positioning and inserting our neuroprobe in a laboratory test system. A block diagram of the complete test system is shown in Fig. 7. The system was designed not only to test the hybrid neuroprobe in its own right (though this was the most important goal), but also to exercise a signal extraction, processing, and transmission system. The output from the hybrid neuroprobe is first directed to a low power analog-to-digital converter (ADC) (40 ksps per channel at 12-bits) controlled by a complex programmable logic device-based programmable timing circuit. The ADC output drives a fiber-optic transmitter that couples the serial data stream (15.36 Mb/s) to a photoreceiver mounted on a second demultiplexer circuit board, the output of which goes into a personal computer (PC) through a National Instruments (Model PCI-6533) high-speed digital input–output board for data storage, display and processing. Making the controllers programmable will simplify protocol changes as we scale up the system for more channels.

Separating the signal processing electronics into two separate boards connected by one or two fiber optic links served two purposes. First, it significantly simplies the laboratory setup for *in vitro* and *in vivo* probing by minimizing board size and cabling requirements adjacent to the probe. Second, its modularity will allow us to test the development of the implantable optical devices for supplying power and returning data that are central to our long-term plan for a complete sensor system. Such optical links are suitable eventually for very high speed data transmission without electromagnetic interference ($>$10 Gb/s) and offer significant advantages for compatibility with biological systems both through material compatibility and through minimizing sites for infection or inflammation.

The integrated neuroprobe was evaluated by first immersing the probe electrodes into a standard ACSF, a physiological saline solution with resistivity ranging 0.5–1 $\mathrm{k\Omega \cdot cm}$. An AgCl coated silver electrode was also immersed in the saline bath a few cm away from the probe set to act as the reference electrode. By applying a small sinusoidal voltage at 1.5 kHz between this common electrode and the amplifier circuit, we could test all the silicon microelectrode probes simultaneously. An example of these results is shown in Fig. 8, which shows the system output voltage recorded at the PC for three different levels of excitation. While the gain and noise performance of the stand-alone CMOS chip have already been detailed

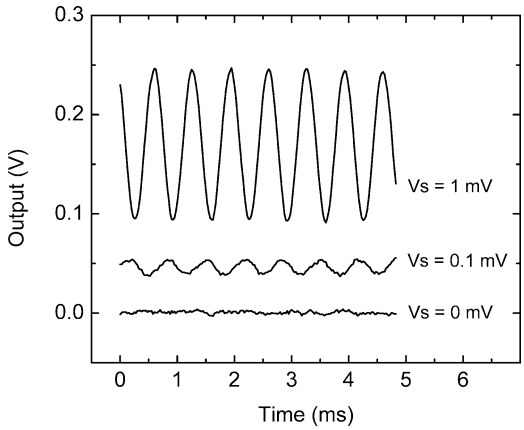

Fig. 8. Amplifier output for 1.5-kHz sinusoidal excitation in saline solution, showing response relative to the base noise level ($\mathrm{V_s = 0\ mV}$). Levels of 0.1 and 1 mV roughly correspond to action potential and local field potential excitation levels, respectively (dc levels were arbitrarily adjusted for clarity).

in Section II of this paper, the usefulness of these results is that we were able to measure directly the gain and the noise level of the preamplifiers under semi-realistic conditions that might apply to *in vivo* recording, including the contribution to noise levels from the probes themselves after processing for encapsulation. The results showed that the hybrid integrated unit had an average gain of 44 dB and an root mean square (rms) noise, relative to the input of the preamplifier circuit, of approximately 9 μV including the contribution from the probes themselves, values quite close to the design expectations.

In a second set of proof-of-concept experiments, we employed the multielectrode integrated neuroprobe in *in vitro* experiments on thalamocortical brain slices from rats [16]. Sprague-Dawley rats of age 13–17 days postnatal were decapitated under anesthesia, and their brains were quickly removed and placed in ice-cold, oxygenated ACSF containing (in millimoles): 126 NaCl, 3 KCl, 126 NaCl, 3 KCl, 1.25 $\mathrm{NaH_2PO_4}$, 2 $\mathrm{MgSO_4}$, 26 $\mathrm{NaHCO_3}$, 10 dextrose, and 2 $\mathrm{CaCl_2}$. Approximately 400-μm-thick thalamocortical slices were prepared with a Leica VT 1000S vibratome. Then, slices were incubated for 45 min at 32 °C in a holding chamber filled with ACSF saturated with 95% $\mathrm{O_2}$/5% $\mathrm{CO_2}$. Afterwards, the slices are kept in this holding chamber at room temperature until they are transferred to a submersion-type recording chamber. After transferring the prepared slice to the recording chamber, the Pt/PtSi coated tips of the microelectrode array were inserted into the barrel cortex region of the brain slice at a depth of approximately 200 μm, under precise control with a three-axis micromanipulator. Recordings are made at room temperature with continuous replenishment of oxygenated ACSF containing 10 μmol picrotoxin in solution.

With the bath application of picrotoxin, we could chemically induce spontaneous neural activity in the brain slices, whose telltale signature of local field potential activity is shown in Fig. 9, recorded from one typical electrode. Rhythmic oscillatory field potentials were measured with a signal amplitude approximately 0.5 mV and the period of the neural activity in the range of 80–120 ms, which is consistent with the result recorded by conventional laboratory systems using an ACSF-filled glass pipette electrode. We verified that all the 16 electrodes and channels were functional. These *in vitro* results thereby suggest that

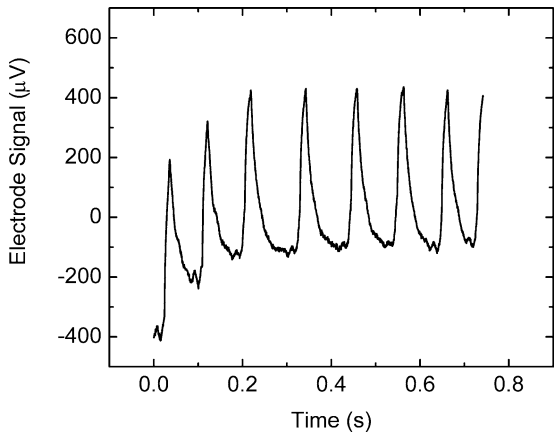

Fig. 9. Typical recording of the oscillatory local field potential response in a thalamocortical brain slice of a rat induced by bath application of picrotoxin.

the hybrid neuroprobe assembly with our particular integration strategy offers a performance comparable to that of the present conventional laboratory neural recording systems, and that this approach can be applied to practical biological subjects *in vivo* with further miniaturization and optimization.

One significant challenge for *in vivo* applications, which the present work has yet to address, concerns encapsulation approaches and their evaluation for chronic biological implants. A search for encapsulation materials and techniques for chronic implants ranges from traditional glass-metal seals [16] to polymer stereolithography [17], with consideration given to silicones, epoxies, and fluoropolymers with and without additional parylene coatings [18], [19]. The criteria that need to be met include biocompatibility, electrical isolation, material isolation, and mechanical strength [20]. These issues have been an area of active research since the development of the pacemaker in the 1950s [21], [23]. The implant of active bio-sensors adds to the constraints by requiring electrical isolation of potentials measured in volts rather than the millivolts usually measured by passive sensors and these potential differences are both within the encapsulated system and between parts of that system and the surrounding fluid medium. The typical shortest dimension of neural implants does not exceed 5 mm, which limits the thickness of encapsulants.

Recognizing the difficulty of this problem, our initial approach, still at early beginning stages, has been to develop short-term solutions that allow the main focus of this research to advance. On these terms, a successful encapsulation has integrity measured in days rather than years. We have used devices encapsulated as described above in an ongoing series of experiments. Microscopic examination and electrical testing after the measurements reported in this paper did not reveal any signs of degradation. However, as noted, the demands placed by chronic implants require a longer term research program, which we are mounting in parallel with efforts toward further microminiaturization and development of an implantable chip-scale neural recording system.

IV. Summary and Discussion

In this paper we have described the development of a functional "neuroport" and its performance, where a very low power/low noise CMOS preamplifier and integral multiplexer chip has been integrated to a silicon-based microelectrode neural probe array. This versatile and compact hybrid device can be readily scaled to much larger arrays (100 elements and beyond) without a significant thermal load in a brain tissue environment, based on our conservative estimates of the modest heat budgets involved. There are different developmental pathways along which our device technology can advance contemporary neuroprosthesis applications. For example, it may be attractive to employ the present probe as an implantable unit with a transcutaneous micro cable providing a direct electrical interconnection to nearby extracranial electronics. At the same time, the design and implementation of very low power ADC with integrated laser driver and control logic is underway in our laboratory with the view toward embedding all the key functional recording electronics on a second hybrid assembly, as part of a single implant. In this case, the anticipated high digital signal data rates call for critical evaluation of the choice for telemetry that can supply the necessary broad bandwidth for data transmission, and be compatible with the stringent physiological requirements within the skull of test animals, and eventually of human subjects. One such scheme, which we are designing, envisions hybridizing suitable optoelectronic components with an ADC on an implantable microminiaturized platform to perform the functions of the "ADC Board" block of Fig. 7. The digitized electronic signals would be transmitted from the head of a patient optically by a low loss fiber to another location in the body, where noninvasive transcutaneous telemetry and power delivery can be implemented practically.

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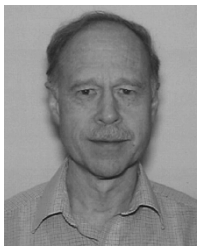

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