Proceedings of the 26th Annual International Conference of the IEEE EMBS
San Francisco, CA, USA • September 1-5, 2004

Development of an Integrated Microelectrode/Microelectronic Device for Brain Implantable Neuroengineering Applications

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Abstract—**An ultra-low power analog CMOS chip and a silicon based microelectrode array have been fully integrated to a microminiaturized "neuroport" for brain implantable neuroengineering applications. The CMOS IC included preamplifier and multiplexing circuitry, and a hybrid flip-chip bonding technique was developed to fabricate a functional , encapsulated microminiaturized neuroprobe device. As a proof-of-concept demonstration, we have measured local field potentials from thalamocortical brain slices of rats, suggesting that the new neuroport can form a prime platform for the development of a microminiaturized neural interface to the brain in a single implantable unit.**

Keywords—**Neuroprosthesis, brain computer interface, low-noise preamplifier, integrated neural probe array**

I. Introduction

Among the several different approaches to intracortical sensors in the form of microelectrode arrays, a silicon-based monolithic unit with up to 100 Pt/PtSi coated electrodes has been particularly successful in sampling the neural activity in the MI [1]. Chronically implanted, this multielectrode arrangement allows the long term (> 1 year) exploration of a significant amount of motor cortex space so that, in conjunction with newly developed decoding techniques using probabilistic analysis [2], good correlation has been achieved for the arm movement of a monkey between the signals recorded directly from the brain ("thought-for-action") and the real physical action by the animal [3]. However, such multielectrode sensors, whether silicon or microwire based, presently require cumbersome, complex cabling arrangements.

While a number of efforts are underway to compact the sensing instrumentation associated with the development of a real-time brain machine interface [4], we show here first steps of a successful integration and operation of a chipscale unit that integrates a silicon-based multielectrode array with an ultra low power, high performance silicon micro-electronic integrated circuit.

This work was supported by the Defense Advanced Research Projects Agency, under the BioInfoMicro porgam (Dr. Eric Eisenstadt). An early version of this work will appear in IEEE Transactions of Biomedical Engineering [10].

The CMOS integrated circuit contains an array of sixteen low-noise preamplifiers with on-board multiplexing and an output buffer amplifier that enable a significant reduction in the amount of wiring which is required to extract the neural signals from the implanted recording unit for subsequent processing and analysis. The amplifier array is bonded directly to a silicon electrode array and then is wire-bonded to a 7-wire interface and encapsulated with silicone. We believe that our hybrid unit represents a first of its kind and, more importantly, view this accomplishment as a prime platform for the development of a next level of microminiaturized "neuroports" where eventually all required electronics will be part of a single brain-implantable unit. We note that earlier successful effort to integrate amplifiers with a sensor probe by Wise and collaborators [5]. This work is based on silicon blade electrodes with side contacts built using anisotropic etching and with the CMOS circuitry at one end of the assembly. Our geometry offers a number of advantages both for implantation and the crtitical considerations for ultra-low power operation.

II. CMOS Integrated Preamplifier Array with Integral Multiplexing

In a CMOS amplifier, one can show that the input-referred thermal noise and power dissipation are inversely related such that the product of noise voltage squared times the power should be constant for a given circuit topology. Recently, Mojarradi and coworkers [6] presented a design that, like our system, is aimed at eventual integration to a set of electrodes. More recently, efforts at Duke University have been presented by Obeid, et al. [7] for integrated circuits to make very small and efficient hybrid head stage systems by incorporating all amplification and filtering operations for 16 channels into single chips. Because of high power dissipation, these circuits seem unlikely candidates for implantation.

In the overall architecture of our CMOS amplifier array the preamplifiers each possess an input bonding pad within its own area of the integrated circuit. We have built our prototypes for a 4×4 microelectrode array (1.6 mm × 1.6 mm), but all designs and fabrication are compatible with the presently standard full 10×10 arrays, and beyond. The amplifier array pitch of 400 μm exactly matches that of the

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array of extracellular electrodes so that bonding each input pad to its corresponding electrode can be done by epoxy ball bonding as outlined in Section III. Each amplifier also has a CMOS transmission gate switch attaching its output to a column line under control of a row select line. Amplifier outputs are routed to the output buffer amplifier by row and column selection implemented with a digital row decoder and an analog column multiplexer also based on CMOS switches. A total of only seven wires is needed as the interface to the chip, including four source select lines, output, power, and ground. The circuit was fabricated on a 2.2 mm × 2.2 mm chip in the AMIS 1.5 μm process.

The individual preamplifiers include an operational amplifier using a folded cascode circuit with P-channel input transistors and a source follower output buffer provides signal amplification. The non-inverting input of that amplifier connects through an RC high-pass network to the sensing electrode that the amplifier services. Gain and high-frequency cutoff are set by a pair of resistors and another polysilicon capacitor in the feedback path. To achieve very large values of resistance in a reasonable area, these feedback resistors were also built with N-MOSFETs, but a circuit that applies a portion of the signal to the gate of one feedback transistor linearizes that resistance to allow its use with large signals. The design target for high frequency cutoff was 7.5 kHz. A separate DC compensation feedback loop sets the bias levels for the amplifier. To isolate the operational amplifier from the effects of the switch connecting the preamplifier to its output column line, there is a P-channel source follower stage implemented in an isolated N-well. Without such isolation, the operational amplifier output would be subject to stepwise disturbance by the inrush current charging the column-line capacitance at the onset of row selection. To conserve power, the bias currents of these followers are only turned on slightly before and during row selection, being controlled by the row select multiplexer.

Our design choices were most heavily constrained by power considerations, which suggested the need to be as near to 50 μW per amplifier as practical so that a scaled-up version would present acceptable thermal loading of the tissue in contact with it (Our worst-case thermal model was 1 degree C temperature rise at the center contact point of the device). **Figure 1** and **Table I** summarize the principal performance parameters of the final design. The measured frequency response from the Bode plot of Figure 4 has -3 dB cutoff points at 10 Hz and 7.3 kHz, and the phase shift at those frequencies is compatible with approximately single pole behavior at both ends of the range. The maximum gain is 44 dB. Table 1 shows the results of SPICE simulation of the amplifier circuitry compared to the measured results. The aggregate noise was measured to be 9 μV_{RMS} referred-to-input from the standard deviation of 0.5 seconds of 40 ksps data taken in saline solution and including thermal noise from the probes.

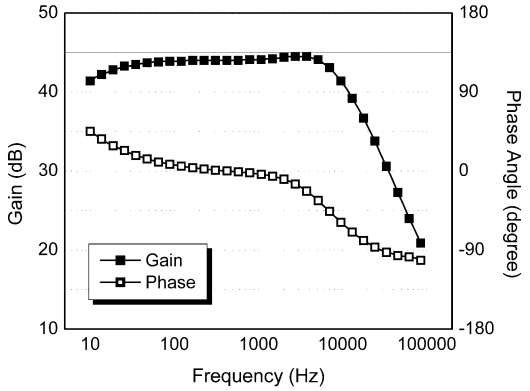

Fig. 1. Bode plot of the response of one channel of the amplifier IC.

TABLE I
SIMULATED AND MEASURED PERFORMANCE OF THE AMPLIFIER IC

Parameter	Simulation	Measurement
Noise (RTI)	6.8 μV_{RMS}	9 μV_{RMS}
Power per amplifier	52 μW	N/A
Power	1.3 mW	1.4 mW
High frequency cutoff (-3 dB)	7.5 kHz	7.3 kHz
Low frequency cutoff (-3 dB)	5 Hz	10 Hz
Overload recovery (200 mV step)	N/A	745 ms

III. PHYSICAL INTEGRATION OF THE MULTIELECTRODE ARRAY WITH CMOS CHIP: A HYBRID NEUROPROBE

We have chosen to use a flip-chip integration strategy based on a carefully chosen conductive epoxy for the the electrical interface between the electrode array and the CMOS chip. This approach has two advantages: first it limits the stresses of pressure and temperature on the base of the electrode array and second, it eliminates the stress that soldering or ultrasonic bonding would place on the double polysilicon input capacitor structure of the chip, increasing its reliability. Conductive silver epoxy (Epotek Model H20E-PFC) is applied to the pads (80 μm × 80 μm) of the CMOS chip by a pin stamping technique so that approximately 150 μm diameter and 50 μm high epoxy dots are deposited with 20 μm placement precision. The 16 element microelectrode arrays were bonded to the CMOS chip by using a high accuracy, manual flip chip and die bonder. Key steps in the process require that the electrode set is first placed on a glass podium, the height of which ultimately fixes the deformation and finished height of the epoxy posts that connect the electrodes to the amplifiers. We used a placement guide made from GaAs plates to hold and align the microelectrode array. The fixture was transferred to the flip chip bonder where its gold base pads are aligned with the pin-stamped epoxy dots on the amplifier IC chip.

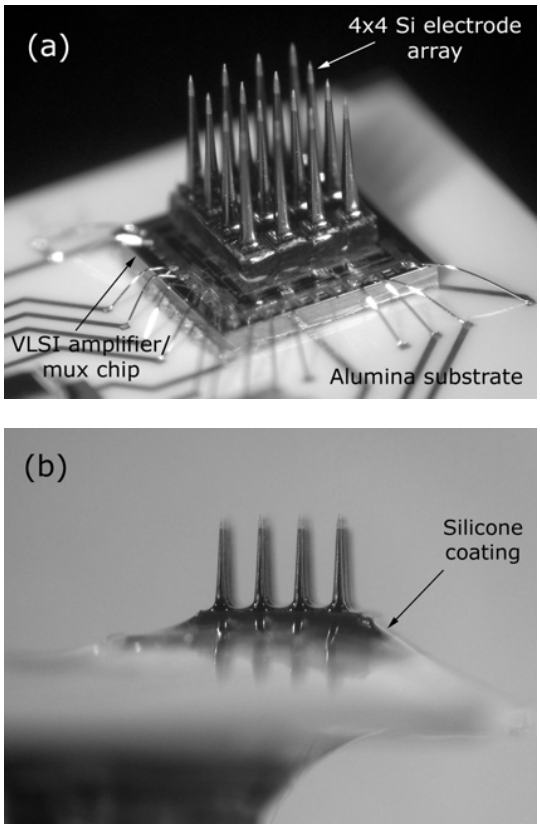

Fig. 2. Electrode and amplifier assembly prior to (a) and after (b) silicone encapsulation.

The two parts were together slowly to a final bonding pressure. Finally, the epoxy was thermally cured. For test purposes, we attached the hybrid neuroprobe by conductive epoxy to a 0.25 mm thick alumina support plate with patterned thin film gold wiring to connect it to the rest of the system electronics and optoelectronics. We emphasize that *the integration approach is fully scalable to large microelectrode arrays (100 recording channels and beyond) and that the choice of a 16 channel system was made for test development purposes only.* **Figure 2** shows a photographic view of the hybrid integrated unit prior to and after the silicone encapsulation.

The integated encapsulated assembly, supported mechanically by the alumina plate, was subsequently mounted to a thin aluminun rod attached to a micromanipulator that enabled positioning and inserting our neuroprobe in a laboratory test system. The system was designed both to test the hybrid neuroprobe and to exercise a signal extraction, processing, and transmission system which included a low power analog-to-digital converter (40 ksps per channel at 12-bits) controlled by a CPLD-based programmable timing circuit. The ADC output drives a fiber-optic transmitter that couples the serial data stream (15.36 Mb/s) to a photoreceiver, the output of which goes into a personal computer (PC) through a National Instruments (Model PCI-6533) high-speed digital IO board for data storage, display and processing. The optical links are suitable eventually for very high speed data transmission without electromagnetic interference (>10 Gb/s) and offer significant advantages for compatibility with biological systems both through material compatibility and through minimizing sites for infection or inflammation.

The integrated neuroprobe was evaluated by several methods, including *in-vitro* experiments on thalamocortical brain slices from rats. With the bath application of picrotoxin, we induced spontaneous neural activity in the brain slices, whose telltale signature of local field potential activity is shown in **Figure 3**, recorded from one typical electrode. Rhythmic oscillatory field potentials were measured with a signal amplitude approximately 0.5 mV and the period of the neural activity in the range of 80-120 ms, which is consistent with the result recorded by conventional laboratory systems using an ACSF-filled glass pipette electrode. We verified that all the 16 electrodes and channels were functional. These *in-vitro* results thereby suggest that the hybrid neuroprobe assembly with our particular integration strategy offers a performance comparable to that of the present conventional laboratory neural recording systems, and that this approach can be applied to practical biological subjects *in-vivo* with further miniaturization and optimization.

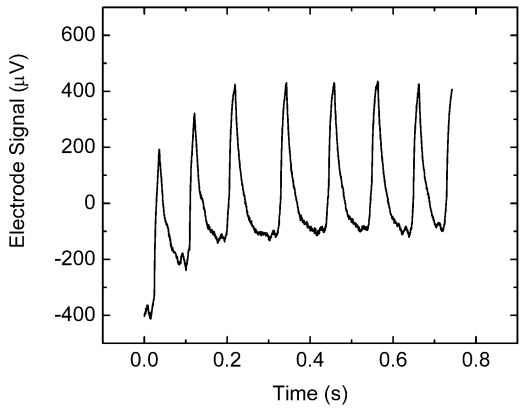

Fig.3. Typical recording of the oscillatory local field potential response in a thalamocortical brain slice of a rat induced by bath application of picrotoxin.

IV. Encapsulation Strategies

Isolating active electronics from exposure to body fluids and the body from potentially harmful materials remains a critical issue in the implementation of chronic neural prosthetics. Neural prosthetics presents unique problems. When designing implants, one likes to exploit the thickness of barrier layers – the thicker the layer, the less likely it is to fail. Unlike other implants, the space into which the device must fit it is limited and the distance between the probe tip

and the electronic circuitry is typically less than a few millimeters. These constraints demand a careful choice of materials and strict attention to the processing. The hybrid neuroprobe described above is an assembly of active and passive components attached to an alumina substrate. Donaldson [8] and Edell [9] have independently suggested/concluded that silicone elastomers are the most viable encapsulant currently available when convenience, compatibility, and ease of processing are factored into the selection.

The short term failure mechanisms are two: pinholes in the coating and voids at electrically active surfaces. Pinholes allow direct communication of fluid to sensitive electronics producing immediate failure. These can usually be avoided by casting (rather than dipping or brushing) the encapsulant. Silicone passes water vapor which can condense in voids in the material. If there are voids coincident with conductors failure will occur, although not as rapidly as with pinholes. To avoid these problems it is essential that the surfaces are free from contaminates and that the preparation and curing of the elastomer proceed with great care.

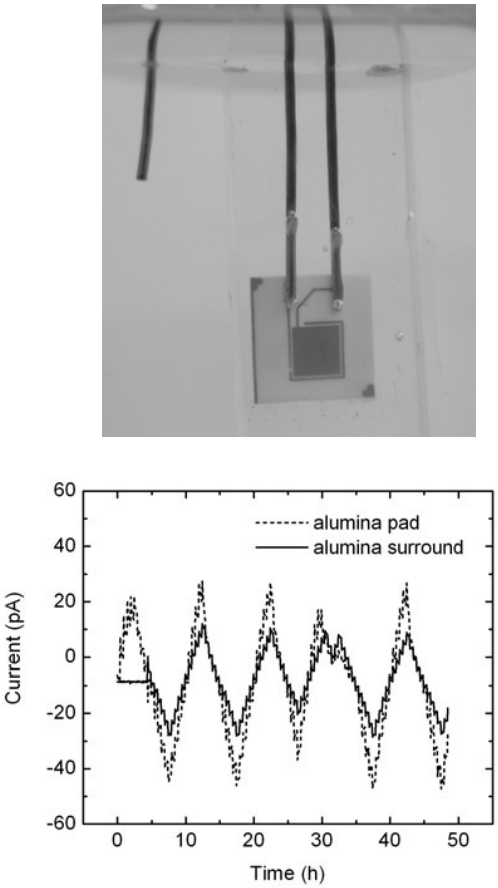

Fig. 4. Upper panel: Alumina substrate with gold conductors encapsulated in silicone in 0.9% saline solution. The other wire is a platinum reference electrode. Lower Panel: Representative data from encapsulation current leakage tests (reference electrode driven, guard ring at ground).

In order to evaluate both materials and processes for chronic neural implants, we have developed a test system that allows fairly rapid discrimination of suitable solutions. The connections in the circuit are flexible allowing a variety of paths for current flow. **Figure 4** shows a one type of test sample, an alumina substrate with two gold conductors. This specimen allows measurement of leakage current across the alumina and through the silicone encapsulant. The current test protocol steps a drive voltage from -5 to +5 VDC in 1 volt increments. The voltage is held for several readings and a corresponding current time plot is shown in Fig. 4 for a representative recent test in our laboratory.

ACKNOWLEDGMENT

The authors wish to thank Dr. I. Ozden and S. Venkataramani for their expertise and participation in the project.

REFERENCES

[1] K. E. Jones, P. K. Campbell, and R. A. Normann, *"A Glass/Silicon Composite Intracortical Electrode Array"*, Annals of Biomedical Engineering, vol. 20, pp. 423-437, 1992.

[2] W. Wu, M. J. Black, D. Mumford, Y. Gao, E. Bienenstock, and J. P. Donoghue, *"A switching Kalman filter model for the motor cortical coding of hand motion"*, Proc. IEEE EMBS, Cancun, Sept. 2003.

[3] M. D. Serruya, N. G. Hatsopoulos, L. Paninski, M. R. Fellows, and J. P. Donoghue, *"Instant neural control of a movement signal"*, Nature, vol. 416, pp. 141–142, 2002.

[4] D. R. Kipke, R. J. Vetter, J. C. Williams, and J. F. Hetke, *"Silicon-substrate intracortical microelectrode arrays for long-term recording of neuronal spike activity in cerebral cortex"*, IEEE Transactions on Neural Systems and Rehabilitation Engineering, vol. 11, pp. 151 –155, June 2003.

[5] R. H. Olsson, III, M. N. Gulari, and K. D. Wise, *"Silicon neural recording arrays with on-chip electronics for in-vivo data acquisition"*, 2nd Annual International IEEE-EMB Special Topic Conference on Microtechnologies in Medicine & Biology, 2-4 May 2002, pp. 237–240.

[6] M. Mojarradi, D. Binkley, B. Blalock, R. Andersen, N. Uslhoefer, T. Johnson, L. Del Castillo, *"A miniaturized neuroprosthesis suitable for implantation into the brain"*, IEEE on Neural Systems and Rehabilitation Engineering, vol. 11, pp 38-42, Mar. 2003.

[7] I. Obeid, J. C. Morizio, K. A. Moxon, M. A. L. Nicolelis, P. D. Wolf, *"Two Multichannel Integrated Circuits for Neural Recording and Signal Processing"*, IEEE Trans. Biomedical Engineering, vol. 50, pp 255–258, Feb. 2003.

[8] P. E. K. Donaldson, *"The essential role played by adhesion in the technology of neurological prostheses"*, Int. J. Adhesion and Adhesives 16 (1996) 105-107

[9] David Edell, Inner Sea Technologies, private communication

[10] W. R. Patterson, Y.-K. Song C. W. Bull, A. P. Deangelis, C. Lay, J. L. McKay, A. V. Nurmikko, J. D. Donoghue, and B. W. Connors "A Microelectrode/Microelectronic Hybrid Device for Brain Implantable Neuroprosthesic Applications", IEEE Trans. Biomedical Engineering, vol. 51, June 2004, in press.